FILING DATE

IF APPROPRIATE

MENT OF COMMERCE APPLICATION NO. ATTY. DOCKET NO. FORM PTO-1449 RADEMARK OFFICE 09/758,970 (REV.7-80) 500395.02 APPLICANT(S) INFORMATION DISCL **EMENT** Ronnie M. Harrison (Use several street FILING DATE **GROUP ART UNIT** 12819- 78/6 January 9, 2001 **U.S. PATENT DOCUMENTS** SUBCLASS CLASS NAME *EXAMINER DOCUMENT NUMBER DATE INITIAL 375 106 Davis et al. 4,984,255 01/08/91 331 1 A 5,315,269 05/24/94 Fujii ΑB 375 373 11/19/96 Zenno et al. 5,577,079 AC 02/15/00 Duffy et al. 375 376 6,026,134 AD 5 327 6,087,857 07/11/00 Wang ΑE 6 Yoshiba 716 6,253,360 B1 06/26/01 ΑF 375 Gaudet 6,285,726 B1 09/04/01 AG ΑH ΑJ Technology Center 2100 ΑJ

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANS	LATION		
						YES	NO		
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		VIHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
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* EXAMINER:

Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. 500395.02

APPLICATION NO. 09/758,970

INFORMATION DISCLOSURE STATEMENT

APPLICANTS
Ronnie M. Harrison

APR 3:0 2001

(Use several sheets if necessary)

FILING DATE
January 9, 2001

GROUP ART UNIT 28/6

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	SE SE		U.S	. PATENT DOCUMENTS				
INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIAT	
HIN	AA	3,633,174	01/04/72	Griffin_	340	172.5	*	
1.	AB	4,077,016	02/28/78	Sanders et al.	331	4	: 	
	AC	4,096,402	06/20/78	Schroeder et al.	307	362		
	AD	4,404,474	09/13/83	Dingwall	307	260		
	AE	4,481,625	11/06/84	Roberts et al.	370	85		
	AF	4,508,983	04/02/85	Allgood et al.	307	577		
	AG	4,511,846	04/16/85	Nagy et al.	328	164		
	АН	4,514,647	04/30/85	Shoji	307	269		
	AI	4,524,448	06/18/85	Hullwegen	375	118		
	ΑJ	4,573,017	02/25/86	Levine	327	114		
	AK	4,600,895	07/15/86	Landsman	331	1 A		
	AL	4,603,320	07/29/86	Farago	341	89		
	АМ	. 4,638,187	01/20/87	Boler et al.	307	451		
	AN	4,638,451	01/20/87	Hester et al.	395	889		
	ΑО	4,687,951	08/18/87	McElroy	307	269		
	AP	4,773,085	09/20/88	Cordell	375	120		
	AQ	4,789,796	12/06/88	Foss	307	443		
	AR	4,818,995	04/04/89	Takahashi et al.	341	94		
	AS	4,893,087	01/09/90	Davis	328	14		
	ΑТ	4,902,986	02/20/90	Lesmeister	331	25		
	ΑU	4,953,128	08/28/90	Kawai et al.	365	194		
	ΑV	4,958,088	09/18/90	Farah-Bakhsh et al.	307	443		
	AW	4,972,470	11/20/90	Farago	380	3		
	AX	4,984,204	01/08/91	Sato et al.	365	189.11		
,	AY	5,020,023	05/28/91	Smith	364	900		
V	ΑZ	5,038,115	08/06/91	Myers et al.	331	2		
XAMINE	R	Ai L. No	01/1/2	DATE CONSIDERE	Dalleal	20		

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FORM PTO-1449 (REV.7-80)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE ATTY. DOCKET NO. 500395.02

APPLICATION NO. 09/758,970

APPLICANTS

Ronnie M. Harrison

FILING DATE

GROUP ART UNIT 28
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OF GREATION DISCLOSURE STATEMENT

z AP	R 3.0	200a	X97			January 9, 2001		Not Yet Assi	gned
13				U.S.	PATENT I	DOCUMENTS			
· No.	DEP.	K G	DOCUMENT NUMBER	DATE		NAME	CLAS	SUBCLASS	FILING DATE IF APPROPRIATE
#	N	BA	5,075,569	12/24/91	Branson		307	270	
		ВВ	5,086,500	02/04/92	Greub		395	550	
		вс	5,087,828	02/11/92	Sato et al.		307	269	
		BD	5,122,690	06/16/92	Bianchi		307	475	
		BE	5,128,560	07/07/92	Chern et a	1.	307	475	
		BF	5,128,563	07/07/92	Hush et al	·	307	482	
		BG	5,134,311	07/28/92	Biber et al	.	307	270	
		вн	5,150,186	09/22/92	Pinney et	al.	357	42	
		BI	5,165,046	11/17/92	Hesson		307	270	
		ВЈ	5,179,298	01/12/93	Hirano et	al.	307	443	
		BK	5,194,765	03/16/93	Dunlop et	al.	307	443	
		ВL	5,212,601	05/18/93	Wilson		360	51	
		ВМ	5,220,208	06/15/93	Schenck		307	443	
		BN	5,223,755	06/29/93	Richley		307	603	
		во	5,233,314	08/03/93	McDermo	tt et al.	331	17	
	L_	BP	5,233,564	08/03/93	Ohshima o	et al.	365	230.05	
		BQ	5,239,206	08/24/93	Yanai		307	272.2	
	·	BR	5,243,703	09/07/93	Farmwald	et al.	395	325	
		BS	5,254,883	10/19/93	Horowitz	et al.	307	443	
		вт	5,256,989	10/26/93	Parker et a	al.	331	1 A	
		ΒU	5,257,294	10/26/93	Pinto et al	<u>. </u>	375	120	
		BV	5,268,639	12/07/93	Gasbarro	et al.	324	158 R	
		вw	5,272,729	12/21/93	Bechade e	et al.	375	118	
		вх	5,274,276	12/28/93	Casper et	al.	307	443	
	1/	BY	5,276,642	01/04/94	Lee		365	189.04	
	\mathbb{V}	BZ	5,278,460	01/11/94	Casper		307	296.5	
EXA	MINI	ER /	HA L. K	160 VA	~/ ⁻]	DATE CONSIDERED	11/	29/04	

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* EXAMINER:

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FILING DATE

GROUP ART UNIT 281

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EXAMINEM	~ OF	3	U.S	. PATENT DOCUMENTS			
EXAMPLE (NITIAL)		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIAT
SIN T	CA	5,281,865	01/25/94	Yamashita et al.	307	279	
	СВ	5,283,631	02/01/94	Koerner et al.	307	451	
	œ	5,289,580	02/22/94	Latif et al.	395	275	····-
	CD	5,295,164	03/15/94	Yamamura	375	120	
	CE	5,304,952	04/19/94	Quiet et al.	331	1 A	
	CF	5,311,481	05/10/94	Casper et al.	365	230.06	
	cc	5,311,483	05/10/94	Takasugi	365	233	
	СН	5,313,431	05/17/94	Uruma et al.	365	230.05	
	СІ	5,315,388	05/24/94	Shen et al.	348	718	
	CJ	5,321,368	06/14/94	Hoelzle	328	63	
	ск	5,337,285	08/09/94	Ware et al.	365	227	
	CL	5,341,405	08/23/94	Mallard, Jr.	375	120	
	СМ	5,347,177	09/13/94	Lipp	307	443	
	CN	5,347,179	09/13/94	Casper et al.	307	451	
	co	5,355,391	10/11/94	Horowitz et al.	375	36	
	СР	5,361,002	11/1/94	Casper	327	530	
	CQ	5,367,649	11/22/94	Cedar	395	375	
	CR	5,379,299	01/03/95	Schwartz	370	108	
	cs	5,390,308	02/14/95	Ware et al.	395	400	
	ст	5,400,283	03/21/95	Raad	365	203	
	CU	5,402,389	03/28/95	Flannagan et al.	365	233	
	cv	5,408,640	04/18/95	MacIntyre et al.	395	550	
	cw	5,410,263	04/25/95	Waizman	327	141	
	сх	5,416,436	05/16/95	Rainard	327	270	
1/	CY	5,416,909	05/16/95	Long et al.	395	275	
$_{\mathbb{V}}_{_}$			05/30/95	Ishibashi	331	11	
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• EXAMINER:

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FORM PTO-1449 (REV.7-80)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

FORMATION DISCLOSURE STATEMENT

ATTY, DOCKET NO. 500395.02

APPLICATION NO. 09/758,970

APPLICANTS

Ronnie M. Harrison

FILING DATE

GROUP ART UNIT Not Yet Assigned

(Use several sheets if necessary) January 9, 2001

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APR 3.	A STATE	7		. PATENT DOCUMENTS	CLASS	SUBCLASS	FILING DATE
INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	IF APPROPRIAT
HON.	DA	5,428,311	06/27/95	McClure	327	276	
1_	DB	5,428,317	06/27/95	Sanchez et al.	331	1 A	
	DC	5,430,408	07/04/95	Ovens et al.	327	407	
	DD	5,430,676	07/04/95	Ware et al.	365	189.02	
	DE	5,432,823	07/11/95	Gasbarro et al.	375	356	
	DF	5,438,545	08/01/95	Sim	365	189.05	
	DG	5,440,260	08/08/95	Hayashi et al.	327	278	
	DH	5,440,514	08/08/95	Flannagan et al.	365	194	
	DI	5,444,667	08/22/95	Obara	365	233	
	נם	5,446,696	08/29/95	Ware et al.	365	222	
	DK	5,448,193	09/05/95	Baumert et al.	327	156	
	DL	5,451,898	09/19/95	Johnson	327	563	· ·
	DM	5,457,407	10/10/95	Shu et al.	326	30	
	DN	5,465,076	11/07/95	Yamauchi et al.	331	179	
	DO	5,473,274	12/05/95	Reilly et al.	327	159	
	DP	5,473,575	12/05/95	Farmwald et al.	365	230.06	
	DQ	5,473,639	12/05/95	Lee et al.	375	376	
	DR	5,485,490	01/16/96	Leung et al.	375	371	
	DS	5,488,321	01/30/96	Johnson	327	66	·
	DT	5,489,864	02/06/96	Ashuri	327	161	
	טם	5,497,127	03/05/96	Sauer	331	17	
	DV	5,498,990	03/12/96	Leung et al.	327	323	
	DW	5,500,808	03/19/96	Wang	364	578	
	DX	5,506,814	04/09/96	Hush et al.	365	230.03	
1/	DY	5,508,638	04/16/96	Cowles et al.	326	38	•
V	DZ	5,513,327	04/30/96	/Farmwald et al.	395	309	

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ATTY. DOCKET NO. 500395.02

APPLICATION NO. 09/758,970

APPLICANTS

Ronnie M. Harrison

FILING DATE

GROUP ART UNIT 281

-Not Yet Assigned January 9, 2001 APR 3.9 7000 **U.S. PATENT DOCUMENTS** SUBCLASS NAME CLASS FILING DATE DOCUMENT NUMBER DATE IF APPROPRIATE 345 114 07/02/96 Knapp et al. 5,532,714 327 150 5,539,345 07/23/96 Hawkins EB 230.08 365 Zagar et al. 08/06/96 5,544,124 EC 375 376 5,544,203 08/06/96 Casasanta et al. ED 327 159 5,552,727 09/03/96 Nakao EE 395 800 Parkinson et al. 09/17/96 5,555,429 EF 327 115 09/17/96 Wright et al. 5,557,224 EG 550 395 09/17/96 Stones et al. 5,557,781 EH 408 Tsukada 327 10/08/96 5,563,546 ΕI 327 172 Curran et al. 5,568,075 10/22/96 EJ 199 Sato et al. 327 10/22/96 5,568,077 375 376 Aoki 5,572,557 11/05/96 395 555 11/05/96 Vogley 5,572,722 EM 365 230.06 5,574,698 11/12/96 Raad EN 327 94 Farwell 11/19/96 5,576,645 EO 395 551 Johnson et al. 5,577,236 11/19/96 ĒΡ 326 30 Dillon et al. 11/26/96 5,578,940 EQ Sher et al. 326 34 11/26/96 5,578,941 ER 61 371 5,579,326 11/26/96 **McClure** ES 326 30 Motley et al. 12/03/96 ET 5,581,197 327 276 5,589,788 12/31/96 Goto ΕU 365 185.08 Arakawa et al. 12/31/96 5,590,073 EΥ Rothenberger et al. 365 189.01 01/14/97 5,594,690 EW 327 158 5,614,855 03/25/97 Lee et al. EX 365 238.5 04/08/97 Hotta 5,619,473 EY 65 327 04/15/97 Lee et al. 5,621,340

EXAMINER

HAI L. NOUYEN

DATE CONSIDERED

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FORM PTO-1449 (REV.7-80)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

FINE ORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY, DOCKET NO. 500395.02

APPLICATION NO. 09/758.970

APPLICANTS

Ronnie M. Harrison

FILING DATE

GROUP ART UNIT

Not Yet Assigned January 9, 2001 **U.S. PATENT DOCUMENTS** FILING DATE CLASS SUBCLASS DATE DOCUMENT NUMBER 365 200 04/15/97 Jungroth et al. 5,621,690 22.1 371 Sine et al. 04/15/97 FB 5,621,739 365 185.09 05/06/97 Malhi 5,627,780 FC 365 222 Wright et al. 05/06/97 5,627,791 FD 227 365 05/20/97 Naritake et al. 5,631,872 FE 233 365 Furutani et al. 5,636,163 06/03/97 FF 230.03 365 Schaefer 06/03/97 FG 5,636,173 230.03 365 06/03/97 Rao 5,636,174 365 230.03 Akiyama et al. 06/10/97 5,638,335 365 233 07/08/97 Ohno et al. 5,646,904 FJ 93 326 Ashuri FΚ 5,652,530 07/29/97 230.05 365 Hush et al. 08/12/97 5,657,289 FL 395 551 Farmwald et al. 5,657,481 08/12/97 FM 365 233 09/02/97 Pascucci et al. 5,663,921 FN 233 365 09/09/97 Conkle 5,666,322 FO 365 200 Fujioka et al. 09/16/97 FP 5,668,763 233 365 09/16/97 Furatani 5,668,774 FO 327 158 Kobayashi et al. 10/07/97 5,675,274 Jeddeloh et al. 395 551 11/25/97 5,692,165 327 108 Hamasaki et al. 5,694,065 12/02/97 FT 365 233 X **Iwamoto** 5,708,611 01/13/98 FU 327 12 01/27/98 Baumgartner et al. 5,712,580 F۷ 327 12 02/17/98 Daly 5,719,508 FW 233 04/14/98 Uchida 365 5,740,123 FX 120 368 5,751,665 05/12/98 Tanoi FY 327 159 5,767,715 06/16/98 Marquis et al. DATE CONSIDERED **EXAMINER**

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FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
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PATENT AND TRADEMARK OFFICE

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ATTY. DOCKET NO. APPLICATION NO. 500395.02 09/758,970

APPLICANTS

Ronnie M. Harrison

FILING DATE
January 9, 2001

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XAMINER INITIAL \		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIAT
KIN	GA	5,768,177	06/16/98	Sakuragi	365	194	
1	GB	5,778,214	07/07/98	Taya et al.	395	551	
	GC	5,781,499	07/14/98	Koshikawa	365	233	
	GD	5,784,422	07/21/98	Heermann	375	355	
	GE	5,789,947	08/04/98	Sato	327	3	
	GF	5,790,612	08/04/98	Chengson et al.	375	373	
	GG	5,794,020	08/11/98	Tanaka et al.	395	552	
	GН	5,805,931	09/08/98	Morzano et al.	395	884	
	GI	5,812,619	09/22/98	Runaldue	375	376	
	G	5,822,314	10/13/98	Chater-Lea	370	337	
	GK	5,831,929	11/03/98	Manning	365	233	•
	GL	5,841,707	11/24/98	Cline et al.	365	194	
	GM	5,852,378	12/22/98	Keeth	. 327	171	
	GN	5,872,959	02/16/99	Nguyen et al.	395	552	
	GO	5,889,829	03/30/99	Chiao et al.	375	376	
	GP	5,898,674	04/27/99	Mawhinney et al.	370	247	
	GQ	5,917,760	06/29/99	Millar	365	194	
	GR	5,920,518	07/06/99	Harrison et al.	365	233	
	GS	5,926,047	07/20/99	Harrison	327	159	
	GT	5,926,436	07/20/99	Toda et al.	365	236	
	GU	5,940,608	08/17/99	Manning	395	551	
	GV	5,940,609	08/17/99	Harrison	395	559	
	GW	5,946,244	08/31/99	Manning	365	194	
	GX	5,953,284	09/14/99	Baker et al.	365	233	
	GY	5,964,884	10/12/99	Partovi et al.	713	503	
V	GZ	5,990,719	11/23/99	Dai et al.	327	244	
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	a Neve	arm.	ATION DISCLOSU	RE STATEM	ENT	APPLICANTS Ronnie M. Harrison				
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JEXAMI WITH	NER	oric	DOCUMENT NUMBER	DATE		NAME	CLAS	S SUBCLASS	FILING IF APPRO	DATE
#1	ブ	НА	6,005,823	12/21/99	Martin et	al.	365	230.08		
Ī		нв	6,011,732	01/04/00	Harrison e	et al.	365	194		
		нс	6,016,282	01/18/00	Keeth		365	233		
		НD	6,026,050	02/15/00	Baker et al.		635	233		
		HE	6,029,250	02/22/00	Keeth		713	400		
		HF	6,038,219	03/14/00	Mawhinne	ey et al.	370	242		
- 1		HG	6,067,592	05/23/00	Farmwald	et al.	710	104		
		нн	6,101,152	08/08/00	Farmwald	et al.	365			
		н	6,101,197	08/08/00	Keeth et a	l	370	517		
	,	HU	6,105,157	08/15/00	Miller		714	744		
V		нк	6,160,423	12/12/00	Haq		327	41		
				FORE	GN PATEN	T DOCUMENTS				
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ļ		/							YES	NO
HL		HL	0 171 720 A2	02/19/86	EP				X	
HI.	N	нм	6-1237512	10/22/86	JP (Abstra	act Only)			X	
X		HN	0 295 515 A1	12/21/88	EP				Х	
	,	но	2-112317	4/25/90	JP (+ Abs	tract)				X
		HP	0 406 786 A1	1/9/91	EP				х	
	,	HQ	0 450 871 A2	10/9/91	EP				х	
		HR	0 476 585 A3	3/25/92	EP		ļ		<u>X</u>	_
	_	-HS	4-135311	5/8/92	JP (+ Abs	tract)				_X
,,		HT	5-136664	6/1/93	JP (+ Abs	tract)				_X
	,-	HU	5-282868	10/29/93	JP (Abstra	act Only)			X	
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\not	0	INK	DRM	ATION DISCLOSU	RE STATEM	ENT	APPLICANTS Ronnie M. Harrison			
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Ł,	7	K	31/2	0 655 741 A2	5/31/95	EP			Х	
Y	PADE	ZN	нх	0 655 834 A1	5/31/95	EP			х	
	WO 95/22200 8/17/95 PC			PCT			x			
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	th	W,	ΙB	0-7319577	12/8/95	JP (Abstra	act Only)		x	
٩	HL	N	ıc	0 703 663 A1	3/27/96	EP			x	
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							; Author, Title, Date, Pertinent Page			
	1	_		Alvarez, J. et	al. "A Wide	e-Bandwidt	h Low Voltage PLL for E-78. No. 6, June 1995,	PowerPC TM Mi	croprocesso	ors''
F	7	_	נו	l I			4M X 16 SLDRAM Pip		nk 25 V	
		\$.	IK_	Operation," S	SLDRAM C	onsortium	Advance Sheet, published	ed throughout the	e United Sta	ites,
-			 	pp.1-22	"Draft Stan	dard for a F	High-Speed Memory Int	erface (Syncl in		
			IL	Microproces	sor and Mici	rocomputer	Standards Subcommitte	ee of the IEEE C	omputer	
		~	 			by the Insti	tute of Electrical and El	lectronics Engine	ers, Inc., No	ew
\vdash		I		York, NY, pp Anonymous,	"Programm	able Pulse	Generator", IBM Techn	ical Disclosure E	Bulletin, Vol	l.
		,	IM_	17, No. 12, N						
\vdash	Anonymous, "Pulse Combining Network", IBM Technical Disclosure Bulletin, Vol. 32, No.									
	12, May 1990, pp. 149-151									
卜	Anonymous, "Variable Delay Digital Circuit", IBM Technical Disclosure Bulletin, Vol. 35,									
	No. 4A, September 1992, pp. 365-366									
T	EXAMINER DATE CONSIDERED									
	t	TAT	` -	L. NOUY	EN		11/29	704		
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	.•		OTHER PRIOR ART (Including	Author, Title, Date, Pertinent Pages, Etc.)			
VA.	DEMARI		Arai, Y. et al., "A CMOS Four Chan	annel x 1K Time Memory LSI with 1-ns/b Resolution",				
A	1-1-	╍┼╌	IEEE Journal of Solid-State Circuits		arch, 1992, No. 3, New			
4		_	York, US, pp. 359-364 and pp. 528-	531				
			Arai, Y. et al., "A Time Digitizer CM	AOS Gate-Array with a 250	ps Time Resolution", XP			
1		? -	000597207, IEEE Journal of Solid-S	tate Circuits, Vol. 31, No.2,	February 1996, pp. 212-			
		_ _	220		CONTROL OF VOITER			
			Aviram, A. et al., "OBTAINING HIG					
1 1		R.	SPECIAL PAPER WITH A RESIST					
-		_	Disclosure Bulletin, Vol. 27, No. 5,					
			Bazes, M., "Two Novel Fully Comp	iementary Self-Blased Civic	OS Differential Amplifiers,			
	15	\$ T	IEEE Journal of Solid-State Circuits	, voi. 20, No. 2, rebruary 1	991, pp. 103-108			
		$\overline{}$	Chapman, J. et al., "A Low-Cost Hig	h-Performance CMOS Tim	ing Vernier for ATE", IEEE			
1 1	N9		International Test Conference, Paper					
					<u> </u>			
			Cho, J. "Digitally-Controlled PLL w		dechanism for Error			
	It	0	Correction", ISSCC 1997, Paper No.	. SA 20.3, pp. 334-335				
		_	Clinia Y WA TAAAAA TTIA	Deceletion CMOS Timing	Conceptor Pasad on an			
			Christiansen, J., "An Integrated High Array of Delay Locked Loops", IEE	E Lournal of Calid State Cir	wite Vol 31 No 7 July			
	1	- -		E-Journal of Solid-State Circ	cuits, voi. 51, 140. 7, sury			
		\dashv	1996, pp. 952-957 Combes, M. et al., "A Portable Clock	k Multiplier Generator Usin	g Digital CMOS Standard			
			Cells", IEEE Journal of Solid State (
	5 T	"	- Series , IEEE southar of Sond States	onound, 7 on 51, 110. 7, 5 un	, 1550, pp. 500 500			
		\dashv	Donnelly, K. et al., "A 660 MB/s Int	erface Megacell Portable Ci	rcuit in 0.3 μm-0.7 μm			
		<u>. </u>	CMOS ASIC", IEEE Journal of Soli					
	"	`	pp. 1995-2001		· ·			
	+	\top	Goto, J. et al., "A PLL-Based Progra	mmable Clock Generator w	ith 50- to 350-MHz			
	<u>-</u> +	- -	Oscillating Range for Video Signal I					
17			12, December 1994, pp. 1951-1956					
111	. ,//	_	Gustavsion, David B., et al., "IEEE S		ent Interface (SCI)," IEEE			
147	$\mathcal{A} \mid_{\mathrm{IZ}}$	z	Computer Society, IEEE Std. 1596-1					
- '			Hamamata T "AOO MHa Dondam	Column Operating CDD AM	Techniques with Self Skew			
ال	, .		Hamamoto, T., "400-MHz Random	Column Operating SDRAIM	In 5 May 1998 nn 770			
1 7	Compensation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 770-778							
<u> </u>		\dashv	Ishibashi, A. et al., 'High-Speed Clo	ck Distribution Architecture	Employing PLL for 0.6um			
×	_	_	CMOS SOG", IEEE Custom Integra					
$\lfloor \mathcal{A}$	Ji	ВТ						
1.1		\top	Kim, B. et al., "A 30MHz High-Spee	ed Analog/Digital PLL in 21	ım CMOS", ISSCC,			
>	$\in \uparrow$	ct	February 1990					
EVA	MINIED			DATE CONSIDERED				
CAA	MINER	41	i L. NOUYEN	11	129 10Cl			
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OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.) Kikuchi, S. et al., "A GATE-ARRAY-BASED 666MHz VLSI TEST SYSTEM", IEEE International Test Conference, Pager 21.1, 1995, pp. 451-458 Ko, U. et al., "A 30-ps JITTER, 3.6-µs LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE-ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4 Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No-FA 18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Niclson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps litter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Sacki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S.	OM	PON!	ATION DISCLOSURE STATEMENT					
CHER PRIOR ART (including Author, Tite, Date, Pertinent Pages, Etc.) Kikuchi, S. et al., "A GATE-ARRAY-BASED 666MHz VLSI TEST SYSTEM", IEEE International Test Conference, Paper 2T.1, 1995, pp. 451-458 KO, U. et al., "A 30-ps JITTER, 3.6-us LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE-ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4 Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb.500MB/s DRAM", IEEE International State Circuits Conference Digest of Technical Papers, Paper No-RA 18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Liushin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Niclson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps itter", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1995, pp. 1259-1266 Sacki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", TEBER Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1655 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1556-1655 Santos, D. et al., "A 700-Mb/s/pin-CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 481-49 SEXAMINER: Initial Internace considered, whether up	/ APR 3.0	2001 E	(Use several sheets if necessary)		Not Yet Assigned			
International Test Conference, Paper 21.1, 1995, pp. 451-458 Ko, U. et al., "A 30-ps JITTER, 3.6-µs LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE-ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4 Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No-FA 18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Ligustin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Niclson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1995, pp. 289-291 Shirotori, T. et al., "A 20-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Si	To the state of th		OTHER PRIOR ART (Including	ng Author, Title, Date, Pertinent Pages, Etc.)				
Ko, U. et al., "A 30-ps ITTER, 3.6-µs LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE-ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4 Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No-FA 18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Lijustin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1733-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 SEXAMINER: Initial if reference considered, whether or not criteria is in conformance with MFEP 609. Draw line through/diation if not in	PADEM							
GATE ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23:3.1-23.3.4 Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No. FA. 18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16-2, 1991, pp. 426-429 Ljuslin, C. et al., "An Integrated 16-channel GMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps litter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Sacki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994	*	JD	International Test Conference, Pape	TZT.1, 1995, pp. 451-458				
International Solid-State Circuits Conference Digest of Technical Papers, Paper NoFA 18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium-on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Tournal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A Z00-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial interace considered, whether or not criteria is in conformance with MPEP 609. Draw line through/Citation if not in	-	JE	GATE ARRAYS", IEEE Custom Ir	ntegrated Circuits Conference	e, 1993, pp. 23.3.1-23.3.4			
18.6, 1994, pp. 300-301 Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Lipustin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Niclson, E., "Inverting latches make simple VCO", EDN, June 19, 1997								
Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429 Ljustin, C. er al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Niclson, E., "Inverting latches-make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Sacki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin-CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial ir reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through Citation if not in	- 1	JF	1 '	onference Digest of Technica	l Papers, Paper No. FA			
Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches-make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin cMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through Citation if not in			Lesmeister, G., "A DENSELY INT		MANCE CMOS TESTER",			
Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 7993, pp. 625-629 Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in		JG .	International Test Conference, Pape	r 16.2, 1991, pp. 426-429				
Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through clausion if not in		1						
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Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732 Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123 Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997 Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps litter", IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through Citation if not in				dependent DLL and PLL Based on Self-Biased				
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Novof, I. et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter", IEEE Journal of Solid State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signating Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in								
Range and ±50 ps Jitter", IEEE Journal of Solid State Circuits, Vol. 30, No. 11, November 1995, pp. 1259-1266 Sacki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in		JК	Nielson, E., "Inverting latches make	simple VCO", EDN, June 1	9, 1997			
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Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665 Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291 Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50. Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in			-1 1	ccess, 250-MHz, 256-Mb SDRAM with Synchronous				
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Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER *EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in		3,14	Record, Vol. 1, October 1995, pp. 2	89-291				
Sidiropoulos, S. et al., "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER DATE CONSIDERED 1/29/04 * EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in					uffer", 1991 Symposium on			
Integrating Receivers", IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690. Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44 EXAMINER *EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in		jo	VLSI Circuits Digest of Technical F	apers, pp. 49-50.				
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1	JR	0.08-400MHz Operating Range," IE					
		February 8, 1997, pp.332-333	,				
		Soyuer, M. et al., "A Fully Monoliti	hic 1.25GHz CMOS Frequen	ncy Synthesizer", IEEE			
	45	Symposium on VLSI Circuits Diges					
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		Taguchi, M. et al., "A 40-ns 64-Mb	DRAM with 64-b Parallel D	ata Bus Architecture",			
	17	IEEE Journal of Solid-State Circuits	, Vol. 26, No. 11, November	r 1991, pp. 1493-1497			
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	İ	Tanoi, S. et al., "A 250-622 MHz De	eskew and Jitter-Suppressed	Clock Buffer Using a			
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		Tanoi. S. et. al., "A 250-622 MHz D	eskew and Jitter-Suppressed	Clock Buffer Using Two-			
	JV	Loop Architecture", IEEE IEICE Tr					
	"	904	ŕ				
		von Kaenel, V. et al., "A 320 MHz,	1.5 mW @ 1.35 V CMOS P	I.I. for Microprocessor			
		Clock Generation", IEEE Journal of	Colid State Circuits Vol 3	No. 11 November 1996			
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		pp. 1715-1722	141 A1 - 1-4- D-1 D	lation Oran Process and			
		Watson, R. et al., "Clock Buffer Chi	p with Absolute Delay Regi	Hation Over Process and			
	1X-	Environmental Variations", IEEE Co	ustom Integrated Circuits Co	onierence, 1992, pp. 23.2.1-			
		25.2.5					
		Yoshimura, T. et al. "A 622-Mb/s B					
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	AD	5,182,524	01/26/93	Hopkins		330		149		
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	AF	5,497,355	03/05/96	Mills et al		365		230.08		
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